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GB 2161310 A GB 1446629 A GB 1105340 A
US 3882424 A

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(54) Phase modulation signal generator

(57) A phase modulation signal generator has a voltage controlled oscillator (15) operating at a high frequency (f_0) in a phase lock loop which is locked to an external oscillator (17) and to a phase modulation signal (f_i) of lower frequency than the VCO produced by modulating a direct digital synthesiser (DDS) and subjecting the signal to digital to analogue conversion. The lower frequency (f_i) is the difference between the VCO and external oscillator frequency. In this way the VCO provides a phase modulated signal transformed to a higher frequency.

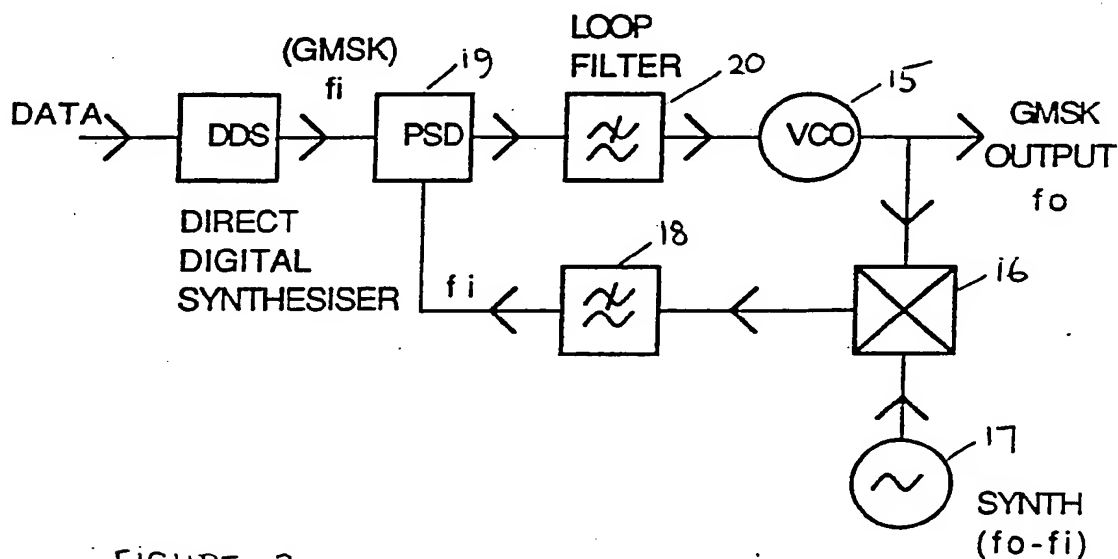


FIGURE 2

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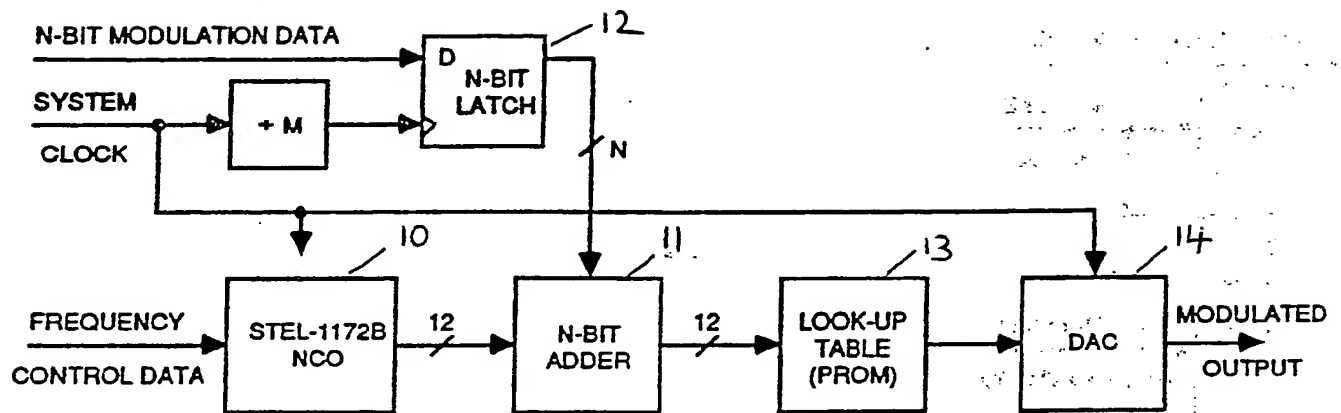


FIGURE 1

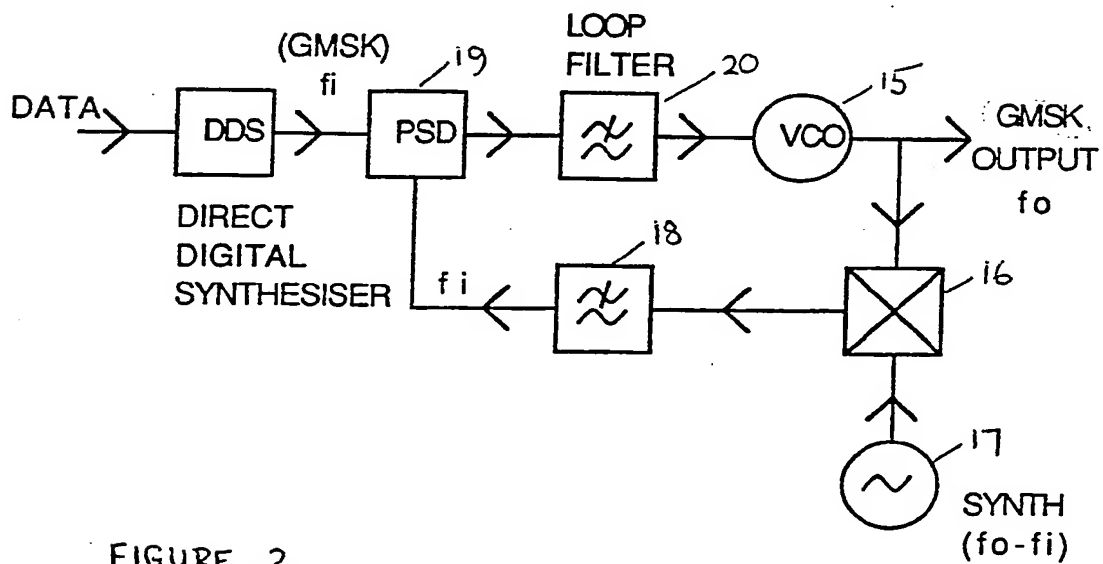


FIGURE 2

Phase Modulation Signal Generator

This invention relates to a phase modulation signal generator and more particularly to a generator capable of producing a stable phase modulation signal of very high frequency such as is required in minimal shift keying (MSK) and Gaussian minimal shift keying (GMSK) signal transmission.

The two most common techniques for generating a GMSK signal are vector modulation and direct modulation of a synthesiser. Vector modulation requires sine and cosine functions of the desired phase modulation to be generated using fast PROMS, which leads to very high power consumption. In addition, the high frequency RF output always contains a residual amplitude modulation component which can lead to gross distortion of the signal when used to drive a class C amplifier with power control. The alternative technique of modulation of a synthesiser requires either : two point modulation (reference oscillator and voltage controlled oscillator) or divider modulation (fractional - N or "Digiphase"). Modulation of a crystal reference oscillator is extremely difficult in terms of obtaining a wide, flat, linear phase modulation response. The accuracy required by GMSK is virtually impossible to achieve. Divider modulation has the drawback of high

spurious levels and high power consumption.

The recent availability of high performance monolithic direct digital synthesisers has enable very accurate GMSK signals to be generated with modest power consumption. However, this is only achieved if the output frequency is low (<5MHz).

The present invention seeks to provide a phase modulation signal generator where at least some of the previously mentioned problems are overcome.

According to the invention there is provided a phase modulation signal generator comprising a voltage controlled oscillator (VCO) operating at a high frequency in a phase lock loop which is locked to an external oscillator of lower frequency and to a phase modulation signal of lower frequency than the VCO produced by modulating a direct digital synthesiser (DDS) and subjecting the signal to digital to analogue conversion, which lower frequency is the difference between the VCO and external oscillator frequency, such that the VCO provides a phase modulated signal transformed to a higher frequency.

In order that the invention and its various other

preferred features may be understood more easily, embodiments thereof will now be described, by way of example only, with reference to the drawings, in which:-

Figure 1 is a schematic block diagram of a known system of direct digital synthesis for producing a phase modulation signal of relatively low frequency, and

Figure 2 is a schematic block diagram of a phase modulation signal generator constructed in accordance with the invention.

The drawing of Figure 1 shows a phase modulation signal generator which employs a numerically controlled oscillator (NCO) 10 for example type STEL-1172B of Stanford Telecommunications Inc. The NCO 10 is operated in the phase mode in which the twelve most significant bits of its phase accumulator are brought out directly to an input of an N-bit adder 11. A modulation signal which may be either a digitised analogue signal or digital data is fed to one input of an N-bit latch 12 driven by a system clock. The output of the latch 12 is coupled to a second input to the adder 11 where it is added arithmetically to the carrier phase signal from NCO 10. The output of the 11 which is the sum of the phases of the NCO and latch output

signals is then routed to a sine lock up table device 13 formed by for example a high speed bipolar PROM such as an 82S321 device. The output from the look up table device 13 is fed to a digital to analogue converter (DAC) 14 the output of which is a phase modulated signal which with such a device can be produced at up to about 20MHz with high stability and modest power consumption.

The present invention is concerned with the production of stable phase modulated signals at much high frequencies employing minimal shift keying (MSK) or Gaussian minimal shift keying at for example 900 MHz and as employed in cellular radio transmissions. In such systems stability is essential or demodulation of the received signal will be impossible.

Referring now to Figure 2 a phase lock loop comprises a voltage controlled oscillator VCO (15) operating at a desired output transmission frequency f_0 , for example 900 MHz, a mixer (16) having an input coupled with the output of VCO 15 and an input coupled with an external synthesiser (17), a low pass filter (18) coupled with the output of the mixer, a phase sensitive detector (PSD) (19) having an input coupled with the output of the low pass filter and a second low pass filter (20) coupled between the output of

the phase sensitive detector (19) and the input to the voltage controlled oscillator (15). A second input to the phase sensitive detector is provided for the output frequency f_i of the digital to analogue converter of the direct digital synthesiser of Figure 1. The frequency of the synthesiser is set to $(f_o - f_i)$ and determines the output frequency.

In operation the output frequency of the voltage controlled oscillator is mixed with a local oscillator frequency produced by the synthesiser 17 to produce a low frequency difference signal at the mixer output which signal is phase compared to the direct digital synthesised input from the digital to analogue converter of Figure 1 and the amplified error signal is used to control the voltage controlled oscillator (15). The voltage controlled oscillator is thereby phase locked to the direct digital synthesised input signal and with a suitable choice of loop gain and bandwidth, e.g. a loop bandwidth of 100KHz, will track the modulation. The phase lock loop has effectively performed a frequency up conversion without the usual concatenation of oscillators, mixers and band pass filters and retains the stability and accuracy of the direct digital synthesised lower frequency.

Although the filters shown are simple low pass filters they can provide a Gaussian frequency characteristic in which case a Gaussian minimal shift keying output signal will be formed from an ordinary minimal shift keying input.

In a specific application for a Gaussian shift modulation cellular radio application, a clock frequency of 13 MHz, output frequency from the digital to analogue converter of 3.25 MHz and data rate of 270 K.bits/sec is employed.

The signal generator is particularly suitable for inclusion in a transmitter/receiver device and such a transmitter receiver is considered to fall within the scope of the present invention. In a particular advantageous application a transmitter/receiver of the time division duplex type can employ the mixer of the phase lock loop to provide a dual function being common to the transmit and receive paths.

CLAIMS

1. A phase modulation signal generator comprising a voltage controlled oscillator (VCO) operating at a high frequency in a phase lock loop which is locked to an external oscillator frequency and to a phase modulation signal of lower frequency than the VCO produced by modulating a direct digital synthesiser (DDS) and subjecting the signal to digital to analogue conversion, which lower frequency is the difference between the VCO and external oscillator frequency, such that the VCO provides a phase modulated signal transformed to a higher frequency.
2. A phase modulation signal generator as claimed in claim 1, wherein the DDS is arranged to provide a low frequency MSK signal such that the VCO provides an MSK signal transformed to a higher frequency.
3. A phase modulation signal generator as claimed in claim 1, wherein the DDS is arranged to provide a lower frequency GMSK signal such that the VCO provides a GMSK signal transformed to a higher frequency.

4. A phase modulation signal generator as claimed in any one of claims 1 to 3, wherein the phase lock loop comprises, in sequence following the VCO, a mixer, a low pass filter, a phase sensitive detector and a second low pass filter coupled to the input of the VCO and wherein the phase sensitive detector has an input coupled to the output of the direct digital synthesiser and the mixer has an input coupled to the external oscillator.
5. A phase modulation signal generator as claimed in any one of claims 1 to 3, wherein the phase lock loop comprises, in sequence following the VCO a mixer, a low pass filter, a phase sensitive detector and a Gaussian filter coupled to the input of the VCO and wherein the phase sensitive detector has an input coupled to the output of the direct digital synthesiser and the mixer has an input coupled to the external oscillator.
6. A phase modulation signal generator as claimed in claim 4 or 5, wherein the local oscillator is a synthesiser.
7. A phase modulation signal generator as claimed in any one of the preceding claims, wherein the loop bandwidth of the phase lock loop is arranged to be of the order 100 KHz.

8. A phase modulation signal generator as claimed in any one of the preceding claims, wherein the direct digital synthesis provides a signal at a frequency up to 20 MHz and the VCO provides an output frequency in the region of 900 MHz.

9. A phase modulation signal generator substantially as described herein with reference to the drawing.

10. A transmitter/receiver incorporating a phase modulation signal generator as claimed in any one of the preceding claims.

11. A transmitter/receiver as claimed in claim 10 of the time division duplex type wherein the mixer of the phase lock loop has a dual function being common to the transmit and receive paths.

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